INTERCARRIER SOUND AMPLIFIER-LIMITER AND DISCRIMINATOR DESIGN FOR TRANSISTOR TV RECEIVERS

By Samuel A. Schwartz

I. INTRODUCTION

The use of the intercarrier system for the sound i-f portion of the television receiver results in circuit simplicity as well as ease of operation. The 4.5 mc intercarrier i-f signal conventionally is taken from a point beyond the second detector in the receiver and amplified to a level suitable for driving an f-m demodulator. It is necessary to prevent any amplitude modulation that may appear on the intercarrier signal from appearing in the demodulated output. Thus, amplitude limiting must be imposed in the amplifier-demodulator configuration.

It is desirable to remove the intercarrier signal ahead of the video amplifier in order to prevent amplitude modulation effects within the amplifier itself, due to the large signal excursions. The intercarrier takeoff point, which provides gain as well as a linear transfer characteristic beyond the second detector, is at the collector of the video driver stage. (See "Video Amplifier Design for Transistor TV Receivers," APP-67.) Under worst conditions the 4.5 mc intercarrier level is 20 millivolts as obtained from a suitably tuned circuit placed in the collector of the video driver transistor. The minimum gain required to raise the intercarrier level suitable to effect adequate limiting action is 30 db.

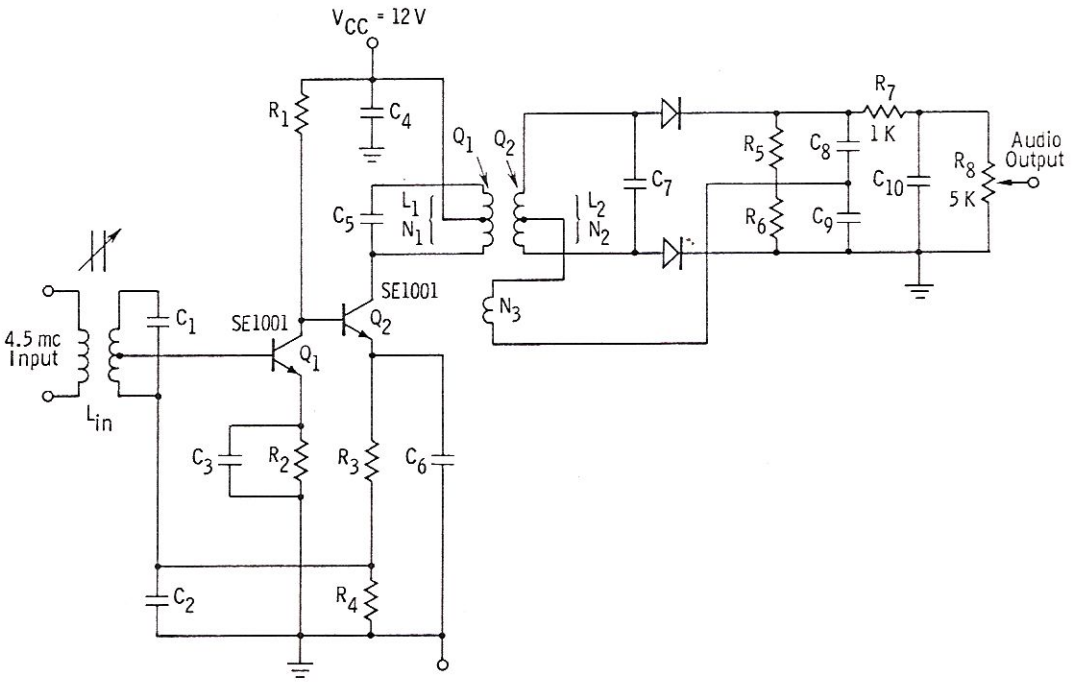

FIG. 1. Schematic diagram of amplifier-limiter and discriminator.

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Amplification of the intercarrier signal can be obtained by using general-purpose silicon planar transistors, such as type SE1001, in conventional circuitry. Amplitude limiting can be accomplished by driving the same type devices into saturation. Therefore, use of a transistor with lower saturation resistance, such as type SE3001, will give slightly better performance.

The use of conventional amplifier circuitry to provide the limiter function results in an undesirable shift in the circuit operating point over the range of input signal levels that may be encountered. An amplifier-limiter circuit is shown in Fig. 1 which stabilizes the operating point by means of d-c feedback and thus provides good limiting action over a wide range of input signal levels. The limiter output signal drives a conventional Foster-Seeley discriminator to provide demodulation of the f-m intercarrier.

II. DISCRIMINATOR DESIGN

The impedance level at which the discriminator operates is low in order to drive the associated audio amplifier circuitry. The load resistors R_5 and R_6 in the discriminator circuit (see Fig. 1) are selected to be compatible with the desired output impedance while effecting an appropriate load on the discriminator transformer and the preceding limiter circuit. A suitable value for the limiter load resistor and thus the primary damping resistance is 1 KΩ. The value of R_5 and R_6 are approximately 4 R_p and thus are each equal to 4 KΩ. A practical transformer design can be obtained by setting the primary "Q" equal to the secondary "Q" (Ref. 1).

$$Q = Q_1 = Q_2$$

The value of "Q" for a center frequency, f_c, of 4.5 mc and a linear range of frequency to amplitude conversion of $2\Delta f$ = 50 kc/0.8 = 62.5 kc * is

$$Q = \frac{f_c}{2\Delta f}$$

$$= \frac{4.5 \times 10^6}{62.5 \times 10^3} = 72 \qquad (2)$$

The secondary damping resistance is approximately equal to the diode load resistor $R_5 = R_6 = R_s$. The secondary tuning capacitor C_7 is determined as follows:

$$C_7 = \frac{Q_2}{\omega_c R_s}$$

$$= \frac{72}{6.28\ (4.5 \times 10^6)\ (4 \times 10^3)}$$

$$= 0.636 \times 10^{-9}$$

$$= 636 \text{ pf} \qquad (3)$$

The value of secondary inductance L_2 must resonate with C_7 at 4.5 mc so that

$$L_2 = 1/4\pi^2 f_c^2 C_7$$

$$= 1/4\pi^2(4.5 \times 10^6)^2 (636 \times 10^{-12})$$

$$= 1.97\ \mu\text{h} \qquad (4)$$

The value of primary inductance L_1' is $L_2/1.77$ = 1.97 μh/1.77 = 1.11 μh which resonates with capacitance C_5' at 4.5 mc.

$$C_5' = L_2 C_7 / L_1'$$

$$= 1.97 \times 10^{-6} \times 636 \times 10^{-12} / 1.11 \times 10^{-6}$$

$$= 1130 \text{ pf} \qquad (5)$$

A more suitable size for the primary tuning capacitor is obtained if the primary inductance L_1' is converted to a step up transformer with the capacitor C_5 across the whole primary winding. The winding can be allowed a step up ratio of 1:2 resulting in a total primary inductance L_1 = 4.44 μh and the tuning capacitor C_5 = 282 pf.

*The discriminator curve is linear for about 80% of its range, so that it is necessary to increase the desired frequency discrimination range accordingly.

The mutual inductance M of the inductances L_1 and L_2 is

$$M = K\sqrt{L_1 L_2}$$

$$K = 1.5/Q$$

$$M = 1.5\sqrt{L_1 L_2})/Q$$

$$= \frac{1.5\sqrt{1.11 \times 10^{-6} \times 1.97 \times 10^{-6}}}{72}$$

$$= 0.0308\ \mu h \qquad (6)$$

The discriminator transformer is constructed such that the above inductance values are satisfied where N_1 and N_3 are wound with N_3 on top of N_1 producing near unity coupling between the two coils.

Capacitors C_8 and C_9 provide adequate bypassing of the frequency f_c but have no effect on the audio output signal. The de-emphasis network consisting of resistors R_7 and volume control R_8 in parallel and capacitor C_{10} has a time constant of approximately 75 microseconds.

III. AMPLIFIER-LIMITER DESIGN

The amplifier-limiter consists of two d-c coupled common-emitter stages. A d-c feedback path from the emitter circuit of the limiter to the base circuit of the amplifier maintains bias stability as well as constant collector current in both stages. Proper bias for both stages is established by suitable choice of the values of resistors R_1, R_2, R_3, and R_4 consistent with the supply voltage V_{CC} (see Appendix).

The values of resistors R_1, R_2, R_3, and R_4 can be calculated from the equations in the Appendix. Having previously established a value of equivalent load resistance of 1 KΩ, a reasonable value of collector current i_{c_2}, which is also consistent with maximizing β, is 5 mA. By also allowing a collector current i_{c_1} of 5 mA in the input stage, r'_e is made sufficiently small to produce a considerable voltage gain at 4.5 mc. The value of V_{CE} (sat) is assumed to be 1 volt at 5 mA. The collector supply voltage V_{CC} is 12 volts and a minimum value for β is 40.

$$R_1 = [0.9\ V_{CC} - 2 - V_{CE}\ (sat)]\,/\,i_{c_1}$$

$$= [0.9\,(12) - 2 - 1]\,/\,5 \times 10^{-3} = 1560\ \Omega \qquad (5A)$$

$$R_2 = 0.1\ V_{CC}/i_{c_1}$$

$$= 0.1\ (12)/5 \times 10^{-3} = 240\ \Omega \qquad (4A)$$

$$R_3 = [0.6 + V_{CE}\ (sat)]\,/\,i_{c_2}$$

$$= [0.6 + 1]/5 \times 10^{-3} = 320\ \Omega \qquad (7A)$$

$$R_4 = [0.1\ V_{CC} + 0.7]\,/\,i_{c_2}$$

$$= [0.1\ (12) + 0.7]\,/\,5 \times 10^{-3} = 380\Omega \qquad (6A)$$

The d-c voltage stabilizing gain of the amplifier is

$$A_V(0) = \frac{R_1[\beta_2(R_3 + R_4)]}{R_2[R_1 + \beta_2(R_3 + R_4)]}$$

$$= \frac{1.56 \times 10^3\,[40\,(320 + 380)]}{240\,[1.56 \times 10^3 + 40\,(320 + 380)]}$$

$$= 6.16 \qquad (7)$$

The d-c feedback ratio B(0) is

$$B(0) = \frac{\beta_1 R_2 R_4}{\beta_1 R_2 R_4 + R_3(\beta_1 R_2 + R_4)}$$

$$= \frac{(40)\,(240)\,(380)}{(40)\,(240)\,(380) + 320\ [(40)\,(240) + 380]}$$

$$= 0.532 \qquad (8)$$

The change in collector current i_{c_2} due to d-c feedback is reduced by the factor $1/[1 + AB]$, and has a numerical value of

$$\frac{1}{1 + AB} = \frac{1}{1 + (6.16)\,(0.532)}$$

$$= 0.234 \qquad (9)$$

A considerable improvement in the over-all d-c regulating ability of the circuit is obtained if R_2 is replaced by a voltage source equal to $(i_{c_2} \cdot R_2)$ or 1.2 volts. This can be simulated by replacing R_2 with two silicon diodes in series. For reasons of economy in commercial applications the resistor R_2 will produce satisfactory results.

The first stage gain at 4.5 mc is given by

$$A_{V_1} = \frac{R_1 \beta_2 I_{e_1}(\text{mA})}{R_1 I_{e_2}(\text{mA}) + 26\,\beta_2}$$

$$= \frac{(1.56 \times 10^3)\,(40)\,(5)}{(1.56 \times 10^3)\,(5) + (26)\,(40)}$$

$$= 35.3 \qquad (10)$$

The second stage gain at 4.5 mc before limiting is

$$A_{V_2} = R_L \Big/ r'_{be}$$

$$= R_L I_e(\text{mA}) \Big/ 26$$

$$= (1 \times 10^3)\,(5) \Big/ 26 = 192 \qquad (11)$$

The voltage gain of the amplifier-limiter before limiting occurs is $A_{V_1} \times A_{V_2} \simeq 7000$. Since the rms output voltage is approximately 5 volts prior to limiting, the required input voltage is slightly less than 1 millivolt, a value considerably smaller than the required minimum.

The input tuned circuit should pass a bandwidth in excess of that designed into the discriminator transformer so that the combined response will not exhibit undesirable bandwidth shrinking. The bandwidth of the input tuned circuit may thus be set to three times the information bandwidth or 150 kc from which the Q_{in} of the input circuit is obtained.

$$Q_{in} = f_c \Big/ B'$$

$$= (4.5 \times 10^{-6}) \Big/ 150 \times 10^3$$

$$= 30 \qquad (12)$$

The input admittance of the general-purpose silicon planar transistor type SE1001 is $g_{ie} = 1.35$ mmhos and $b_{ie} = 1.1$ mmhos from which an equivalent $Q = 0.815$ is obtained. Therefore, in order to realize a $Q = 30$, the total susceptance, b_t, must be increased by 30×1.35 mmhos minus 1.1 mmhos = 39.4 mmhos. The Miller capacitance in the circuit will account for an additional capacitance C_M.

$$C_M = C_{ob}\,(A_{V_1} + 1)$$

$$= 3.5 \times 10^{-12}\,(35.3 + 1)$$

$$= 127 \text{ pf} \qquad (13)$$

The capacitance C_1 required to resonate the input coil is

$$C_1' = \frac{b_t}{2\pi f_c} - C_M$$

$$= \frac{39.4 \times 10^{-3}}{(6.28)\,(4.5 \times 10^6)} - 127 \times 10^{-12}$$

$$= 1273 \text{ pf}$$

The required inductance L'_{in} to resonate with C_1 at 4.5 mc is

$$L'_{in} = 1/4\pi^2 f_c^2\, C_1$$

$$= 1/4\pi^2 (4.5 \times 10^6)^2\, 1.273 \times 10^{-9}$$

$$= 0.984\ \mu\text{h} \qquad (14)$$

The value of C_1' may be reduced to a more practical size by making L'_{in} a step up transformer as was done for the discriminator transformer primary. Again a 1:2 step up ratio is used reducing the size of C_1' to $C_1 = 318$ pf and the value of L'_{in} increases to $L_{in} = 3.93\ \mu$h. The primary winding is wound next to the ac grounded side of L_{in} and has an inductance approximately the same as $L'_{in} = 0.984\ \mu$h.

Capacitors C_2, C_3, C_4, and C_6, which have a value of .01 μf, are used to provide adequate bypassing at the 4.5 mc frequency.

IV. CONCLUSION

A very satisfactory intercarrier amplifier-limiter can be constructed using the Fairchild type SE1001 general-purpose silicon planar transistor. The direct coupled arrangement of the transistors in the circuit given reduces the number of tuned circuits normally employed. The straight forward and simple design procedure which has been described can be extended to encompass f-m 10.7 mc limiter design using similar transistor types. It has been shown that improved limiter performance can be obtained by the use of a voltage reference element within the amplifier-limiter. Such an arrangement is preferred where lowest cost is not an objective.

The Foster-Seeley discriminator gives excellent performance when used with this amplifier-limiter circuit but it is anticipated that the ratio detector would give comparable results with perhaps somewhat degraded linearity.

APPENDIX

The equivalent d-c circuit of the amplifier-limiter is shown in Fig. 1A. The d-c circuit can be arranged as in Fig. 2A where resistor R_2 is replaced by a voltage reference source. The circuit is then the same as that constituting a simple series voltage regulator. The boxed in portions of the schematic represented by dotted lines show the portions of the circuit representing the amplifier gain, A, the feedback circuit, B, and the voltage reference E_{REF}.

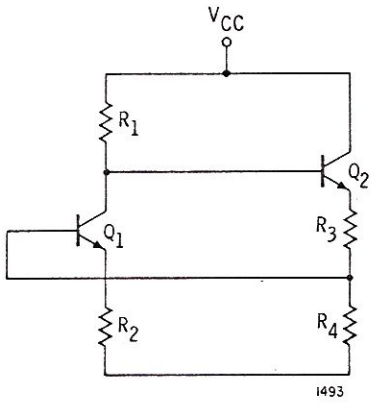


FIG. 1A. D-c circuit of the amplifier-limiter.

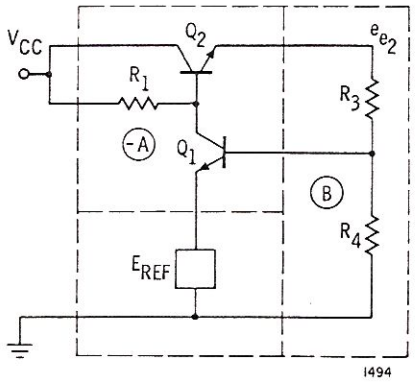


FIG. 2A. Modified d-c circuit of the amplifier-limiter.

The circuit is shown in block form in Fig. 3A for the purpose of analysis. Included in the circuit is a voltage source, E_{os}, which represents an offset in the circuit tending to change the emitter voltage of Q_2. With switch S_1 in position A, the emitter voltage of transistor Q_2 is as follows:

$$e_0 = -A(Be_0 - E_{REF})$$

$$= -A\,Be_0 + A\,E_{REF} \qquad (1A)$$

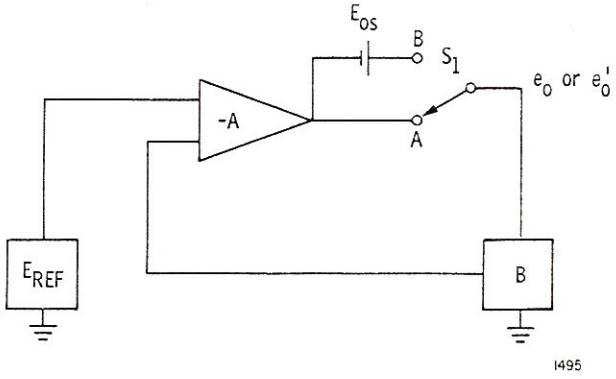


FIG. 3A. Block diagram of the modified amplifier-limiter.

$$e_0 + ABe_0 = AE_{REF}$$

$$e_0(1 + AB) = AE_{REF}$$

$$e_{e_2} = e_0 = AE_{REF} \Big/ (1 + AB) \qquad (2A)$$

The switch S_1 is changed to position B thereby placing the offset voltage E_{os} in series with the amplifier output voltage e_0'.

$$e_0' = -A(Be_0' - E_{REF}) + E_{os}$$

$$= -ABe_0' + AE_{REF} + E_{os}$$

$$e_0' + ABe_0' = AE_{REF} + E_{os}$$

$$e_0'(1 + AB) = AE_{REF} + E_{os}$$

$$e_0' = (AE_{REF} + E_{os}) \Big/ (1 + AB)$$

$$e_{e_2} = e_0'$$

$$= [AE_{REF} \Big/ (1 + AB)] + [E_{os} \Big/ (1 + AB)] \qquad (3A)$$

Equation 2A shows that the emitter voltage of transistor Q_2 is proportional to the reference voltage E_{REF}. Thus, in the actual amplifier-limiter circuit, the voltage across Q_2 being equal to $V_{CC} - e_{e_2}$, is controlled by the reference voltage.

Under the condition of limiting of large signals, Q_2 is driven into saturation resulting in a change of emitter current which attempts to change the emitter voltage e_{e_1} or e_0 in the block diagram. Equation 3A shows that the offset voltage, e_{os}, produced by a change in emitter current is reduced in its effect on the emitter voltage, e_{e_2}, by the factor $1/(1 + AB)$. Thus the degree to which the operating point remains constant depends on the product AB throughout a wide range of limiting levels.

The voltage reference can be replaced by resistor R_2 as shown in Fig. 1A with a consequent reduction in the limiter stability. The emitter resistor causes a gain reduction of the amplifier over that obtained with a voltage reference. The equivalent voltage reference using R_2 becomes equal to $(i_{e_1} \cdot R_2)$ where i_{e_1} is dependent on circuit values as well as collector supply voltage. As a result of these factors the use of an emitter resistor in place of a voltage reference gives inferior limiter performance. A special case exists where R_2 is reduced to zero. The circuit then operates from a voltage reference consisting of the base-emitter diode voltage drop of transistor Q_1.

An amplifier-limiter design using resistor R_2 necessitates a high R_1/R_2 resistance ratio in order to realize appreciable voltage gain. However, consideration of overall bias and available collector supply voltage limits the ratio to a moderate quantity. A reasonable design can be obtained by allowing the emitter voltage of Q_1 to equal $0.1\ V_{CC}$ and the collector emitter voltage of Q_1 = 2 volts plus $V_{CE(sat)}$. Assuming that the base-emitter voltages of Q_1 and Q_2 are equal to 0.7 volts and that base current is negligibly small compared to collector current, the following equations define the circuit resistance values: (Refer to Fig. 1A).

$$i_{c_1} R_2 = 0.1\ V_{CC}$$

$$R_2 = 0.1\ V_{CC} \Big/ i_{c_1} \qquad (4A)$$

$$0.1\ V_{CC} + 2 + V_{CE(sat)} + i_{c_1} R_1 = V_{CC}$$

$$R_1 = \frac{V_{CC} - 0.1\ V_{CC} - 2 - V_{CE(sat)}}{i_{c_1}}$$

$$R_1 = \frac{0.9\ V_{CC} - 2 - V_{CE(sat)}}{i_{c_1}} \qquad (5A)$$

$$i_{c_2} R_4 = 0.1\ V_{CC} + 0.7$$

$$R_4 = (0.1\ V_{CC} + 0.7) \Big/ i_{c_2} \qquad (6A)$$

$$i_{c_2}(R_3 + R_4) + 0.7 = 0.1\ V_{CC} + 2 + V_{CE(sat)}$$

$$R_3 = (0.6 + V_{CE(sat)}) \Big/ i_{c_2} \qquad (7A)$$

The d-c voltage stabilizing gain of the amplifier, assuming unity gain for the emitter follower, is

$$A_V(0) = \frac{R_1[\beta_2(R_3 + R_4)]}{R_2[R_1 + \beta_2(R_3 + R_4)]} \qquad (8A)$$

The d-c feedback ratio B(0) may be expressed as follows:

$$B(0) = \left[\frac{\beta_1 R_2 R_4}{\beta_1 R_2 + R_4}\right] \Big/ \left[\frac{\beta_1 R_2 R_4}{\beta_1 R_2 + R_4} + R_3\right]$$

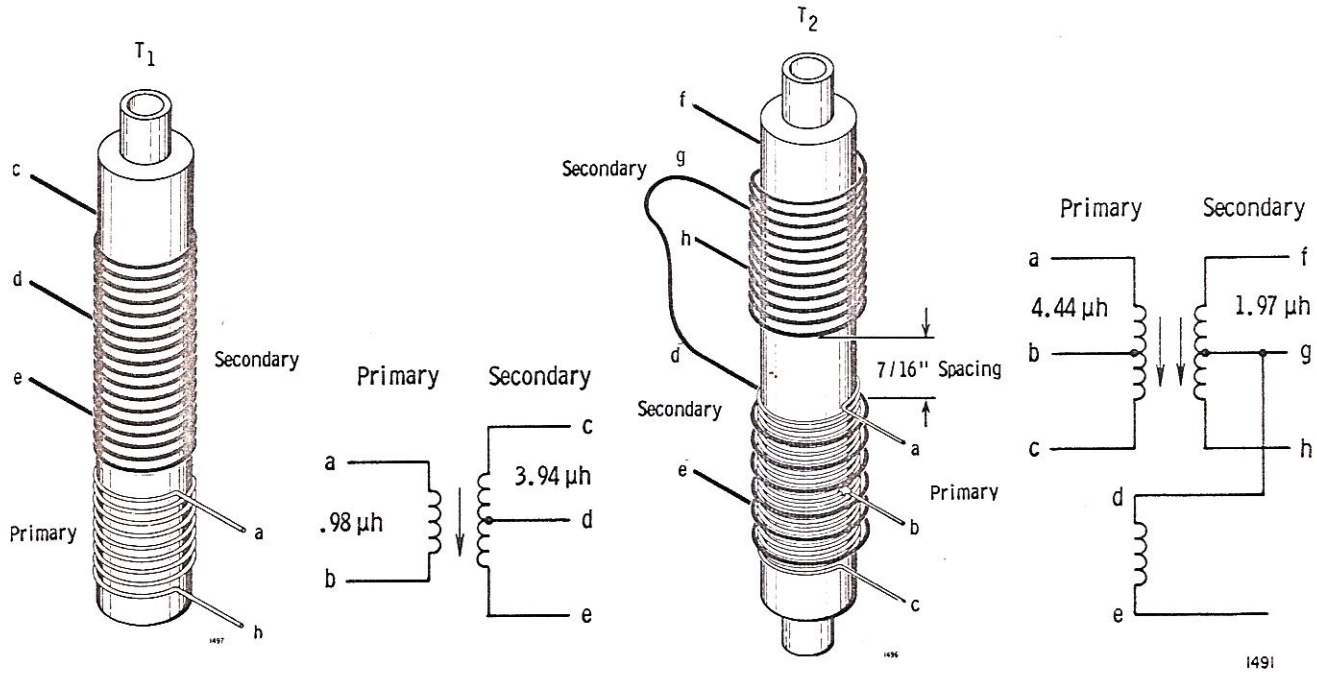
$$B(0) = \frac{\beta_1 R_2 R_4}{\beta_1 R_2 R_4 + R_3(\beta_1 R_2 + R_4)} \qquad (9A)$$

The addition of appropriate load, coupling, and bypass elements to the basic d-c coupled circuit results in high r-f gain with limiting action. The first stage becomes a wideband amplifier with a desired bandwidth restriction imposed by the input tuned circuit. The r-f gain of the first stage can be shown in approximate forms as

$$A_V = \frac{R_1\left[\beta_2 \frac{26}{I_{e_2}(ma)}\right]}{\frac{26}{I_{e_1}}\left[R_1 + B_2 \frac{26}{I_{e_2}(ma)}\right]}$$

$$= \frac{R_1 \beta_2 I_{e_1}(ma)}{R_1 I_{e_2}(ma) + 26\,\beta_2} \qquad (10A)$$

DISCRIMINATOR COIL DATA



PRIMARY = 9 turns #36 nyclad wire.

SECONDARY = 18 turns #36 nyclad wire. Center tapped.

CORE = Miller #30-106.

FORM = 5/16" diameter.
Primary and secondary wound in the same direction side by side.

PRIMARY = 20 turns #36 nyclad wire. Center tapped.

SECONDARY = 12 turns #36 nyclad wire. Center tapped.

SECONDARY d and e = 6 turns #36 nyclad wire.
Overwound in the same direction as primary on primary.

CORE = Miller #30-106.

FORM = 5/16" diameter.

REFERENCE

1. Radiotron Designer's Handbook, Radio Corp. of America.

ACKNOWLEDGMENT

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LIST OF SYMBOLS

$A_V(0)$	D-c voltage stabilizing gain
A_{V_1}	First stage voltage gain
A_{V_2}	Second stage voltage gain
B'	Bandwidth of input tuned circuit
$B(0)$	D-c feedback ratio
C_1	Practical value of capacitor used with input step-up transformer
C_1'	Calculated value of capacitance across input coil
C_5	Practical value of primary tuning capacitor used with step-up transformer in actual circuit
C_5'	Calculated value of primary tuning capacitance
C_M	Miller capacitance
E_{OS}	Offset source voltage
E_{REF}	Voltage reference of limiter equivalent circuit
f_c	Center frequency of bandpass
L_1	Primary inductance
L_1'	Calculated value of primary inductance
L_2	Secondary inductance
L_{in}	Practical value of input inductor
L_{in}'	Calculated value of input inductor
N_1	Total number of primary turns of discriminator coil
N_2	Total number of secondary turns of discriminator coil
N_3	Total number of turns of tertiary coil equal to one-half the secondary turns
Q_1	Primary coil Q
Q_2	Secondary coil Q
Q_{in}	Input tuned circuit Q
R_p	Primary damping resistance
R_s	Secondary damping resistance